IN THE SPECIFICATION

Please amend the specification through the following paragraph substitutions. The specific changes are shown in the following marked-up versions of the original paragraphs.

C1

The sub-title on page 1, line 7 is amended as follows: Related Applications ~~Inventions~~

C2

The paragraph beginning on page 1, line 9 is amended as follows:

The present application ~~invention~~ is related to the following applications ~~inventions~~ which are assigned to the same assignee as the present application ~~invention~~:

C3

The paragraph beginning on page 1, line 11 is amended as follows:

Serial No. 09/631,037~~_____~~, entitled "Electronic Assembly Comprising Substrate with Embedded Capacitors ~~and Methods of Manufacture~~"; and

C4

The paragraph beginning on page 1, line 13 is amended as follows:

Serial No. 09/628,705~~_____~~, entitled "Electronic Assembly Comprising Interposer with Embedded Capacitors and Methods of Manufacture".

C5

The sub-title on page 1, line 16 is amended as follows: Technical Field ~~of the Invention~~

C6

The paragraph beginning on page 1, line 18 is amended as follows:

The present subject matter ~~invention~~ relates generally to electronics packaging. More particularly, the present subject matter ~~invention~~ relates to an electronic assembly that includes a ceramic/organic hybrid substrate having one or more embedded capacitors to reduce switching noise in a high speed integrated circuit, and to manufacturing methods related thereto.

C7

The sub-title on page 1, line 24 is amended as follows: Background Information ~~of the Invention~~

The paragraph beginning on page 3, line 15 is amended as follows:

C8 FIG. 1 is a block diagram of an electronic system incorporating at least one electronic assembly with embedded capacitors in accordance with one embodiment of the subject matter ~~invention~~;

The paragraph beginning on page 3, line 23 is amended as follows:

C9 FIG. 5 is a flow diagram of a method of fabricating a substrate to package a die, in accordance with one embodiment of the subject matter ~~invention~~.

The sub-title on page 3, line 26 is amended as follows: C10 Detailed Description ~~of Embodiments of the Invention~~

The paragraph beginning on page 3, line 28 is amended as follows:

In the following detailed description of embodiments of the subject matter ~~invention~~, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the subject matter ~~inventions~~ may be practiced. C11 These embodiments are described in sufficient detail to enable those skilled in the art to practice them ~~the invention~~, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present subject matter ~~inventions~~. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiment of the present subject matter ~~invention~~ is defined only by the appended claims.

The paragraph beginning on page 4, line 6 is amended as follows:

C12 The present subject matter ~~invention~~ provides a solution to power delivery problems that are associated with prior art packaging of integrated circuits that operate at high clock speeds and high power levels by embedding one or more decoupling capacitors in a multilayer substrate. Various embodiments are illustrated and described herein. In one embodiment, an IC die or chip is directly mounted to a hybrid organic/ceramic multilayer substrate, of which a ceramic portion

C12 (cncl'd)

contains one or more embedded capacitors, and of which an organic portion includes suitable routing and fan-out of power, ground, and signal conductors.

The paragraph beginning on page 4, line 28 is amended as follows:

C13

FIG. 1 is a block diagram of an electronic system 1 incorporating at least one electronic assembly 4 with embedded capacitors in accordance with one embodiment of the subject matter ~~invention~~. Electronic system 1 is merely one example of an electronic system in which the present subject matter ~~invention~~ can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

The paragraph beginning on page 5, line 29 is amended as follows:

C14

FIG. 2 illustrates a top-view of a die 60 on a substrate 50, in accordance with one embodiment of the subject matter ~~invention~~. This die/substrate structure can form part of electronic assembly 4 shown in FIG. 1. Die 60 can be of any type. In one embodiment, die 60 is a processor.

The paragraph beginning on page 6, line 19 is amended as follows:

C15

While an embodiment is shown in which signal traces are provided around the periphery and Vcc and Vss traces are provided at the die core, the subject matter ~~invention~~ is equally applicable to embodiments where signal traces occur other than at the periphery, and to embodiments where Vcc and Vss traces are provided anywhere on the die.

The paragraph beginning on page 6, line 23 is amended as follows:

C16

Further, the present subject matter ~~invention~~ is not to be construed as limited to use in C4 packages, and it can be used with any other type of IC package where the herein-described features of the present subject matter ~~invention~~ provide an advantage.

The paragraph beginning on page 6, line 26 is amended as follows:

C17

FIG. 3 illustrates a cross-section of the die/substrate structure of FIG. 2 taken along line 70 of FIG. 2, in accordance with one embodiment of the subject matter ~~invention~~. The multilayer substrate comprises an organic portion 80 and a ceramic portion 90. One important purpose of the subject matter ~~invention~~ is to provide relatively high capacitance, for example in the form of one or more capacitors embedded in ceramic portion 90, relatively close to the die in order to reduce the effect of reactive inductive coupling when the IC is operating, particularly at high clock speeds.

The paragraph beginning on page 8, line 1 is amended as follows:

C18

Ceramic portion 90, in one embodiment, comprises a plurality of ceramic layers 91-95. Embedded within ceramic layers 91-95, a single capacitor is illustrated, for the sake of simplicity of illustration and description, that includes a first pair of connected plates 141 at Vcc potential and a second pair of connected plates 151 at Vss potential. Between the plates 141 and 151 is an insulating layer of a high permittivity material.

The paragraph beginning on page 9, line 9 is amended as follows:

C19

The particular geometry of the embedded capacitors is very flexible in terms of the orientation, size, number, location, and composition of their constituent elements. One or more discrete capacitors could be used instead of the capacitive structure illustrated in FIG. 3. Reference may be made to Related Applications ~~Inventions~~ 1 and 2 above for further details on the structure and composition of the embedded capacitors.

The paragraph beginning on page 10, line 6 is amended as follows:

C20

In FIG. 3, the conductive plates 141 and 151 comprise conductive layers formed at the boundary between adjoining insulating layers of ceramic material. For example, a first pair of conductive plates 141 are formed between ceramic layers 91/92 and 93/94, and a second pair of conductive plates 151 are formed between ceramic layers 92/93 and 94/95. The first pair of conductive plates 141 are joined by via 143, and they are coupled to Vcc. The second pair of

C20 cancel

conductive plates 151 are joined by via 153, and they are coupled to Vss. Conductive plates 141 and 151 can extend, if desired, throughout substantially the entire region between adjoining layers of ceramic material.

On page 10, between lines 13 and 14, insert the following two paragraphs:

C21

Still referring to FIG. 3, via 143 that electrically couples conductive layers or plates 141 will be seen to penetrate and pass through an adjacent one of the second pair of conductive plates 151 without electrically contacting same. Similarly, via 153 that electrically couples conductive layers or plates 151 will be seen to penetrate an adjacent one of the first pair of conductive plates 141 without electrically contacting it.

With further reference to an embodiment shown in FIG. 3, via 143 is perpendicular to and has a geometrical projection upon either or both of the first pair of conductive layers or plates 141. This geometrical projection of via 143 is surrounded by the corresponding conductive plate 141. That is, the conductive plate extends in every direction from the location where the via 143 contacts the plate 141. Similarly, via 153 is perpendicular to and has a geometrical projection upon either or both of the second pair of conductive layers or plates 151. This geometrical projection of via 153 is surrounded by the corresponding conductive plate 151.

The paragraph beginning on page 10, line 29 is amended as follows:

C22

FIGS. 2-4 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 2-4 are intended to illustrate various implementations of the subject matter that ~~invention, which~~ can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning on page 11, line 21 is amended as follows:

C23

Multilayer stacks of high Dk ply can be used in ceramic portion 50. High Dk ply is commercially available for fabricating ceramic chip capacitors, for example. Suitable high Dk materials, such as titanate particles, can be inserted into the conventional ceramic matrix.

C23 cont'd

Multilayer stacks of high Dk ply, such as $BaTiO_3$, in the present subject matter ~~invention~~ can provide capacitances as high as 10 μF/sq. cm.

The paragraph beginning on page 12, line 9 is amended as follows:

C24

FIG. 5 is a flow diagram of a method of fabricating a substrate to package a die, in accordance with one embodiment of the subject matter ~~invention~~. According to this method, a ceramic/organic hybrid substrate having at least one embedded capacitor is fabricated. The method begins at 251.

The paragraph beginning on page 14, line 3 is amended as follows:

The present subject matter ~~invention~~ provides for an electronic assembly and methods of manufacture thereof that minimize problems, such as switching noise, associated with high clock frequencies and high power delivery. The present subject matter ~~invention~~ provides scalable high capacitance (e.g. >10 mF/square centimeter) by employing one or more embedded decoupling capacitors having low inductance which can satisfy the power delivery requirements of, for example, high performance processors. By using a thin organic portion for conductor routing, the ceramic portion that comprises the decoupling capacitors can be positioned relatively close to the IC die, thus minimizing the inductance. The ceramic portion lends itself well to the fabrication of high valued embedded capacitors and also provides requisite stiffening to the package to prevent warpage. An electronic system that incorporates the present subject matter ~~invention~~ can operate reliably at higher clock frequencies and is therefore more commercially attractive.

C25

The paragraph beginning on page 14, line 15 is amended as follows:

C26

As shown herein, the present subject matter ~~invention~~ can be implemented in a number of different embodiments, including a substrate, an electronic assembly, an electronic system, a data processing system, and methods for making a substrate. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, materials, geometries, and dimensions can all be varied to suit particular packaging requirements.

The paragraph beginning on page 14, line 21 is amended as follows:

Although specific embodiments have been illustrated and described herein, any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present subject matter ~~invention~~. Therefore, it is manifestly intended that embodiments of this subject matter ~~invention~~ be limited only by the claims and the equivalents thereof.